3. (Currently Amended) The device of claim 1, wherein:

said single substrate comprising a substrate having said via connectors from said bottom surface to said top surface through said single <u>semiconductor</u> substrate is selected from the group consisting of a silicon-on-insulator (SOI) substrate, a silicon substrate, a polycrystalline silicon substrate, a glass substrate, a plastic substrate, a ceramic substrate, a germanium substrate, a SiGe substrate, a SiC substrate , a sapphire substrate, a quartz substrate, a GaAs substrate, and an InP substrate.

4. (Currently Amended) The device of claim 1, wherein:

said micromirror section additionally comprises at least one addressing electrode controllable by said control circuitry disposed on said bottom surface of said single <u>semiconductor</u> substrate for actuating said micromirror.

5. (Currently Amended) The device of claim 4, additionally comprising:

at least one of said via connectors comprising electrically conductive routing line through said single <u>semiconductor</u> substrate connects said control circuitry to said at least one addressing electrode.

6. (Currently Amended) The device of claim 5, wherein:

said at least one via connector through said single <u>semiconductor</u> substrate comprising a metallization via connector.

7. (Currently Amended) The device of claim 1, wherein:

said single semiconductor substrate additionally comprises an insulating layer between said bottom surface and said top surface to function as a silicon (SOI) on oxide substrate.

8. (Currently Amended) The device of claim 1, wherein:

said micromirror disposed on said top surface of said single semiconductor substrate further comprising a metallic mirror.

9. (Currently Amended) The device of claim 1, wherein:

said micromirror disposed on said top surface of said single semiconductor substrate further comprising a multi-layer dielectric mirror.

10. (Currently Amended) The device of claim 1, wherein:

said micromirror disposed on said top surface of said single semiconductor substrate further comprising a substantially planar reflective side with neither recesses nor protrusions.

11. (Currently Amended) The device of claim 1, wherein:

said micromirror disposed on said top surface of said single semiconductor substrate further comprising a reflective surface having no edges perpendicular to a projection direction of an incident light propagation vector onto said single substrate.

12. (Currently Amended) The device of claim 11, wherein:

said reflective surface of said micromirror disposed on said top surface <u>of said single semiconductor substrate</u> further comprising a polygon-shaped reflective surface.

13. (Previously Presented) The device of claim 12, wherein:

said polygon-shaped reflective surface is selected from the group of reflective surfaces consisting of a rectangle-shaped reflective surface and a hexagon-shaped reflective surface.

14. (Currently Amended). The device of claim 1, wherein:

said micromirror section comprises a torsion hinge disposed underneath and supporting said micromirror support structure; and

said torsion hinge comprising a pair of supporting structures for supporting said torsion hinge on <u>said top surface of</u> said <u>single semiconductor</u> substrate.

15. (Currently Amended) The device of claim 1, wherein:

said micromirror section comprises at least one stopping member <u>disposed on said top surface of said single semiconductor substrate</u> for limiting a rotation of said micromirror.

16. (Previously Presented). The tool of claim 15, wherein:

said at least one stopping member comprises a <u>first</u> stopping member for limiting the rotation of said micromirror in a <u>first</u> direction; and

a <u>second</u> stopping member for limiting the rotation of said micromirror in a direction opposite to said <u>first</u> direction.

17. (Currently Amended) An array of electromechanical micromirror devices comprising:

a single <u>semiconductor</u> substrate with a bottom surface and a top surface opposite said bottom surface;

a control circuitry disposed on said bottom surface of said <u>single semiconductor</u> substrate; and

an array of micromirror sections disposed on said top surface of said single <u>semiconductor</u> substrate wherein each said micromirror section comprises a micromirror; and

at least one support structure for supporting said micromirror and via connectors opened through said single <u>semiconductor</u> substrate for connecting said control circuit to said support structure.

18. (Currently Amended) The array of claim 17, wherein:

said control circuitry disposed on said bottom surface of said <u>single semiconductor</u> substrate comprising a circuit selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits.

19. (Currently Amended) The array of claim 17, wherein:

said single substrate comprising a substrate having said via connectors from said bottom surface to said top surface through said single <u>semiconductor</u> substrate is selected from the group consisting of a silicon-on-insulator (SOI) substrate, a silicon substrate, a polycrystalline silicon substrate, a glass substrate, a plastic substrate, a ceramic substrate, a germanium substrate, a SiGe substrate, a SiC substrate , a sapphire substrate, a quartz substrate, a GaAs substrate, and an InP substrate.

20 (Currently Amended) The array of claim 17, wherein:

said micromirror section disposed on said top surface <u>of said single semiconductor substrate</u> additionally comprises at least one addressing electrode for actuating said micromirror.

21. (Currently Amended) The array of claim 20, additionally comprising:

at least one of said via connectors comprising an electrically conductive routing line through said single semiconductor substrate connects said control circuitry to said at least one addressing electrode of at least one of said micromirror sections.

22. (Currently Amended) The array of claim 21, wherein:

said at least one via connector through said single semiconductor substrate comprising a metallization via connector.

23. (Currently Amended) The array of claim 17, wherein:

said single substrate additionally comprises an insulating layer between said bottom surface and said top surface of said single semiconductor substrate.

24. (Currently Amended) The array of claim 17, wherein:

said micromirror disposed on said top surface of said single semiconductor substrate further comprising a metallic mirror.

25 (Currently Amended) The array of claim 17, wherein:

said micromirror disposed on said top surface of said single semiconductor substrate further comprising a multi-layer dielectric mirror.

26. (Currently Amended) The array of claim 17, wherein:

said micromirror disposed on said top surface of said single semiconductor substrate further comprising a substantially planar reflective side with neither recesses nor protrusions.

27. (Currently Amended) The array of claim 17, wherein:

said micromirror disposed on said top surface of said single semiconductor substrate further comprising a reflective surface having no edges perpendicular to a projection direction of an incident light propagation vector onto said single substrate.

28. (Currently Amended) The array of claim 27, wherein:

said reflective surface of said micromirror disposed on said top surface of said single semiconductor substrate further comprising a polygon-shaped reflective surface.

29 (Previously Presented) The array of claim 28, wherein:

said polygon-shaped reflective surface is selected from the group of reflective surfaces_consisting of a rectangle-shaped reflective surface and a hexagon-shaped reflective surface.

30. (Currently Amended). The array of claim 17, wherein:

said micromirror section comprises a torsion hinge disposed underneath and supporting said micromirror support structure; and

said torsion hinge comprising a pair of supporting structures for supporting said torsion hinge on said <u>single semiconductor</u> substrate.

31 (Currently Amended) The array of claim 17, wherein:

said micromirror section comprises at least one stopping member for limiting a ~~rotation~~ <u>deflection angle</u> of said micromirror.

32 (Currently Amended) 32. The array of claim 17, wherein:

said at least one stopping member comprises a <u>first</u> stopping member for limiting ~~the rotation~~ <u>a first deflection angle</u> of said micromirror in a <u>first</u> direction; and

a second stopping member for limiting ~~the rotation~~ <u>a second deflection angle</u> of said micromirror in a direction opposite to said first direction.

33. (Currently Amended) A spatial light modulator (SLM) comprising an array of electromechanical micromirror devices wherein said micro-mirror devices further comprising:

a single semiconductor substrate with a bottom surface and a top surface opposite said bottom surface;

a control circuitry disposed on said bottom surface of said single semiconductor substrate;

an array of micromirror sections disposed on said top surface of said single semiconductor substrate wherein each said micromirror section comprises a micromirror; and

a support structure for supporting said micromirror and via connectors opened through said single semiconductor substrate for connecting said control circuit to said support structure.

34. (Currently Amended) A method of fabricating an array of electromechanical micromirrors comprising the steps of:

providing a single semiconductor substrate with a bottom surface and a top surface opposite said bottom surface;

forming control circuitry on said bottom surface of said single semiconductor substrate; and

forming a plurality of support structures on said top surface of said single semiconductor substrate and forming a plurality of micromirrors on top of and supported by said support structures and opening via connectors through said single semiconductor substrate for connecting said control circuit to said support structure.

35 (Currently Amended) The method of claim 34, wherein:

said step of forming said control circuitry comprises a step of fabricating on said bottom surface <u>of said single semiconductor substrate</u> said control circuits selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits.

36. (Currently Amended) The method of claim 34, wherein:

said step of providing said single substrate further comprising a step of providing said single <u>semiconductor</u> substrate selected from a group of <u>semiconductor</u> substrates consisting of a silicon-on-insulator (SOI) substrate, a silicon substrate, a polycrystalline silicon substrate, a glass substrate, a plastic substrate, a ceramic substrate, a germanium substrate, a SiGe substrate, a SiC substrate , a sapphire substrate, a quartz substrate, a GaAs substrate, and an InP substrate.

37. (Currently Amended) The method of claim 34, wherein:

said step of forming said micromirrors additionally comprises a step of forming on said top surface <u>of said single semiconductor</u> a plurality of addressing electrodes for actuating said micromirrors.

38 (Currently Amended) The method of claim 37, additionally comprising a step of:

forming a plurality of electrically conductive routing lines as said via connectors through said single semiconductor substrate for connecting said control circuitry to said plurality of addressing electrodes.

39. (Currently Amended) The method of claim 38, wherein said step of:

forming said plurality of electrically conductive routing lines as a metal via connector through said single semiconductor substrate.

40. (Currently Amended) The method of claim 34, wherein:

said step of providing said single substrate further comprising a step of providing a single semiconductor substrate comprises an insulating layer between said bottom surface and said top surface to function as a silicon on oxide semiconductor substrate.

41. (Currently Amended) The method of claim 34, wherein:

said step of forming a plurality of micromirrors comprises a step of forming on said top surface of said single semiconductor substrate a reflective metallic coating on said micromirrors.

42. (Currently Amended) The method of claim 34, wherein:

said step of forming on said top surface <u>of said single semiconductor substrate</u> a plurality of micromirrors comprises a step of forming a reflective multi-layer dielectric coating on said micromirrors.

43. (Currently Amended) The method of claim 34, wherein said step of forming said micromirrors comprises the steps of:

forming on said top surface <u>of said single semiconductor substrate</u> said plurality of micromirror support structures embedded in a sacrificial layer;

planarizing a top surface of said sacrificial layer and said micromirror support structures;

depositing a micromirror material on said top-surface;

patterning said micromirror material to form a plurality of micromirrors; and

removing said sacrificial layer by an etching process.

44. (Currently Amended) 44. The method of claim 43, wherein:

said step of forming said microstructures in said sacrificial layer further comprising a step of forming on said top surface <u>of said single semiconductor substrate</u> said microstructures in a layer composed of a material selected from a group of materials consisting of a photoresist polymer, a silicon oxide, a silicon nitride, a silicon oxynitride, and an amorphous silicon.

45. (Previously Presented) The method of claim 43, wherein:

said step of planarizing said top surface of said sacrificial layer further comprising a step of applying a chemical mechanical polishing (CMP) process.

(Currently Amended) 46. The method of claim 34, wherein said step of forming a plurality of micromirrors comprises a step of:

patterning said micromirrors on said top surface <u>of said single semiconductor substrate</u> to have no edges perpendicular to a projection direction of an incident light propagation vector onto a plane of said single substrate.

(Previously Presented) 47. The method of claim 46, wherein:

said step of patterning said micromirrors further comprising a step of patterning at least one of said micromirrors as a polygon-shaped micromirror.

(Previously Presented) 48. The method of claim 47, wherein:

said step of patterning said polygon-shaped micromirror is a step of patterning said micromirror either as a rectangle-shaped micromirror or a hexagon-shaped micromirror.

(Previously Presented) 49. The method of claim 34, additionally comprising a step of:

forming a torsion hinge for supporting said support structures by forming a hinge support followed by forming a torsion hinge on top of said hinge support.

(Currently Amended) 50. The method of claim 34, additionally comprising a step of:

forming at least one stopping member on said top surface of said single semiconductor substrate for limiting a ~~rotation~~ deflection angle of said micromirror.

51 (Currently Amended) The method of claim 50, wherein said step of forming at least one stopping member comprises:

forming a first stopping member for limiting a ~~rotation~~ deflection angle of said micromirror in a first direction; and

forming a second stopping member for limiting a ~~rotation~~ deflection angle of said micromirror in a second direction opposite to said first direction.

52.(Currently Amended) A method of fabricating an array of electromechanical micromirrors, comprising the steps of:

providing a single silicon-on-insulator substrate with an epitaxial top silicon layer above an insulator layer, supported by a bottom silicon layer;

forming control circuitry directly on said epitaxial top silicon layer;

removing said bottom silicon layer, thereby exposing said insulator layer;

forming a plurality of support structures on a surface of said insulation layer opposite said epitaxial top silicon layer followed by forming a plurality of micromirrors on top of and supported by said support structures.

53. (Previously Presented) The method of claim 52, wherein:

said step of forming said control circuitry comprises a step of fabricating said control circuits selected from a group of circuits consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, and DMOS circuits.

54 (Previously Presented) The method of claim 52, wherein:

said step of removing said bottom silicon layer comprises a step of applying a back-grinding step to remove said bottom silicon layer below said insulation layer.

55. (Previously Presented) The method of claim 52, wherein:

said step of removing said bottom silicon layer comprises a step of applying a chemical mechanical polishing (CMP) step to remove said bottom silicon layer below said insulation layer.

56. (Previously Presented) The method of claim 52 additionally comprises a step of:

forming a plurality of addressing electrodes for actuating said plurality of micromirrors on a surface of said insulation layer opposite said epitaxial top silicon layer.

57 (Previously Presented) The method of claim 56, additionally comprising a step of:

forming a plurality of electrically conductive routing lines for connecting said control circuitry disposed in said epitaxial top silicon layer to said plurality of addressing electrodes disposed <u>below said insulation layer</u>.

58. (Previously Presented) The method of claim 57, wherein said step of forming said plurality of electrically conductive routing lines comprises the steps of:

forming at least one via through said substrate; and

forming a metallization in said via for connecting said control circuitry in said epitaxial top silicon layer to said plurality of addressing electrodes disposed below said insulation layer.

59. (Previously Presented) The method of claim 52, wherein said step of forming said micromirrors the steps of:

forming said plurality of micromirror support structures embedded in a sacrificial layer below said insulation layer opposite said epitaxial top silicon layer;

planarizing a top surface of said sacrificial layer and said micromirror support structures;

depositing a micromirror material on said top-surface of said sacrificial layer;

patterning said micromirror material to form a plurality of micromirrors; and

removing said sacrificial layer by an etching process.

60. (Previously Presented) The method of claim 59, wherein:

said step of planarizing said top surface of said sacrificial layer further comprising a step of applying a chemical mechanical polishing (CMP) process.